Advanced Semiconductor On-State Voltage Measurement Methodology

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***Abstract*—Accurate measurement of ON-resistance of semiconductor devices serves as a key indicator of how various stress factors impact the electrical, thermal, and long-term reliability performance of wide bandgap devices. Monitoring ON-resistance not only offers technical insight into device physics and degradation mechanisms, but is also used as a diagnostic precursor to device failure and aging. This is particularly important for high-voltage, fast-switching devices, such as wide bandgap (WBG) semiconductors, where precise in-situ measurement of ON-resistance during operation is necessary to assess the device's state of health. Such measurements involve monitoring the device current and ON-state voltage with high accuracy and resolution, while ensuring minimal delay and high-voltage blocking capability. Moreover, these measurements should be immune to variations in device temperature and load conditions as much as possible. In this paper, a novel measurement topology based on a cascode current mirror configuration is introduced and analyzed in depth. A detailed analysis of the circuit's operating principles is provided, and the measurement performance is validated through hardware experiments. The proposed approach integrates the strengths of existing measurement techniques while addressing the limitations identified in the literature.**

***Index Terms*—Wide bandgap (WBG), Gallium Nitride (GaN), Silicon Carbide (SiC), ON-resistance measurement, ON-state voltage measurement circuit (OVMC), In-situ measurement capability.**

I. Introduction

THE measurement of ON-resistance, defined as the resistance between the drain and source of a transistor when the device is in the ON state, is an important parameter to monitor to understand various aspects of device performance, reliability, efficiency, and the overall health of semiconductor devices. Accurate measurement of this parameter is particularly important for wide bandgap (WBG) semiconductor devices, which exhibit much lower specific ON-resistance at a given breakdown voltage due to their high critical-field characteristics and superior channel mobility compared to silicon (Si)-based metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) [1], [2]. Monitoring ON-resistance provides helpful insights into a device's thermoelectric performance, state of health, physical phenomena, and informed design for system optimization, making it an essential parameter for further improving semiconductor test and measurement technology [3]–[5].

For instance, evaluating the thermoelectric performance of semiconductor devices involves analyzing factors such as efficiency, power loss, and heat dissipation, especially for power module packaging [6]. Accurate measurement of ON-resistance is important for understanding these aspects because ON-resistance directly impacts the amount of heat generated within the device during current conduction. In addition, precise measurement of this parameter ensures that the devices operate within safe temperature limits [7].

Also, ON-resistance is a correlated indicator of the device's health condition; any significant changes can signal degradation or impending failure [8]. Therefore, monitoring ON-resistance allows for health assessments of semiconductor devices through in-situ observation, enabling the estimation of potential failures, aging, and overall device lifetime [9], [10]. Real-time monitoring of ON-resistance through the Internet of Things (IoT) offers a powerful tool for capturing the long-term degradation behavior of semiconductor devices [11]. If it can be processed in real-time, the measurement of ON-resistance can enable predictive maintenance, allowing for timely interventions before catastrophic failures occur, thereby reducing downtime and maintenance costs [10].

In addition, ON-resistance measurement can be used to relate intrinsic properties of the materials used in semiconductor devices. In particular, GaN high-electron-mobility transistors (HEMTs) suffer from a parasitic phenomenon of increased ON-state resistance during a switching event from its DC or steady-state value, known as dynamic ON-resistance or current collapse [12]–[15]. This phenomenon exhibits elevated ON-resistance compared to the DC ON-resistance during the conduction state after a switching transition. The severity of the trapping is significantly impacted by various operational and environmental parameters [16], [17]. Hence, the ON-state resistance characteristic helps explain phenomena such as charge trapping, dynamic ON-resistance performance [18], and mechanical stresses from thermal cycling [19].

For packaged power modules based on Silicon Carbide (SiC) and IGBTs, the measurement of ON-resistance reveals the impacts of thermal cycling stress caused by the Coefficient of Thermal Expansion (CTE) mismatch on wire bond integrity, indicating potential degradation [20]. These measurements enable a deeper understanding of device physics fundamentals, the assessment of degradation mechanisms under operational conditions, and the development of improved packaging techniques to enhance device longevity.

Lastly, device performance and trade-off studies are facilitated by understanding the materials' ON-resistance, particularly through the use of Figures of Merit (FOM) [21]. This parameter is used to compare the performance of different

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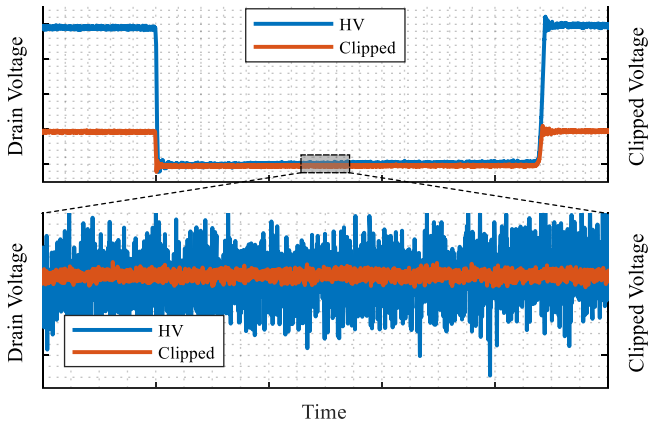


Fig. 1. Illustration of high-voltage switching waveform and clipped-voltage waveform measurement. The bottom panel depicts a close-up view of the two waveforms in the ON-state and highlights the lower resolution of the high-voltage switching waveform compared to the higher resolution data for the clipped voltage measurement, which allows for a more accurate estimation of dynamic ON-resistance during the conduction or ON state.

device materials and architectures [22]. WBG-based devices are often evaluated against traditional Si devices using ON-resistance to highlight their superior performance in high-power, high-frequency switch-mode power applications [23]. Thus, it is a key metric for optimizing device design while investigating the best balance of conductivity, thermal management, and breakdown voltage for overall device performance and efficiency.

In this paper, a novel cascode current-mirror-based ON-state voltage measurement circuit (OVMC) topology is proposed. Accurate, reliable, repeatable, and responsive measurement of ON-resistance is a paramount task due to its relevance to the reasons previously described. However, the development of an accurate and reliable sensing methodology for ON-state voltage or ON-resistance measurement is not trivial [24], [25]; the difficulty of sensing ON-state resistance through measuring the device current and voltage (i.e., Ohm's Law) is augmented when high-voltage operation causes an overdrive of the oscilloscope or acquisition system. Offsetting and expanding a portion of the waveform over a wider range can drive the sampling or acquisition window beyond the dynamic range of the amplifiers and analog-to-digital converters (ADC). This causes the scope's amplifier to saturate and recover from its overdriven condition, resulting in distortions and preventing accurate measurement of the ON-state voltage. Furthermore, the dynamic range of the probe, which is the ratio of the largest to the smallest values of a signal, is based on the resolution of the ADC that samples and converts the measured analog data into digitized data [26]. A challenge exists when the ON-state cannot be adequately captured with a limited number of available bits to sample waveforms during the high-voltage operation of GaN HEMT.

To enable high resolution of detailed ON-resistance data during the conduction state, maintaining a usable effective number of bits during the ON-state to boost vertical resolution is critical. This can be implemented through the use of an ON-state voltage circuit that clips off and limits the high-voltage signal during the OFF-state while providing a high-resolution measurement capability during the ON-state. Fig. 1 illustrates the measurement challenge when a high-voltage switching waveform results in poor resolution quality and low accuracy of data, whereas the clipped voltage waveform provides higher resolution due to a smaller voltage peak required for the probe to measure, thereby increasing accuracy of the ON-state voltage for calculating dynamic ON-resistance.

To cope with the aforementioned ON-state voltage measurement challenge, this paper presents a novel circuit topology, detailing its operation and performance based on various operational conditions, highlighting the circuit's sensing capability over a wide range of switching characteristics using high-voltage WBG devices. The proposed circuit is designed based on a cascode current mirror, which ensures a steady current to minimize measurement sensitivity to the device under test (DUT) operation. This configuration enables high-resolution measurements due to the damping of the measurement peaks during the switching transitions. To enhance the background information, Section II provides a thorough literature survey of the current state-of-the-art (SOA) techniques for measuring ON-state resistance while addressing their limitations. Section III describes the proposed circuit measurement topology along with the operating principles and detailed analysis. Section IV discusses both static and dynamic measurement results across a wide range of test conditions. Lastly, Section V summarizes the key accomplishments enabled by the proposed circuit while addressing the needs for future research endeavors.

II. Technical Review of Prior State-of-the-Art

A variety of clipping or ON-state voltage circuits have been surveyed in the literature. Fig. 2 shows various clipping circuits found in prior art. To provide a performance comparison metric, it is noteworthy to highlight several important aspects of the measurement requirements for WBG transistors: (a) fast dynamic response with small measurement delay, (b) non-loading effects on the device turn-ON or turn-OFF speed, (c) independence from temperature and load currents, (d) small measurement accuracy error, (e) minimal overshoot and undershoot to prevent probe overdrive and maintain high resolution, (f) high bandwidth, and (g) in-situ measurement capability to enable high-voltage continuous switching operation.

Fig. 2(a) topology uses a Zener diode as a peak clipper configuration [27]. During the blocking state, the Zener diode clamps the high-voltage drain bias to a lower clamping voltage level while allowing ON-state voltage measurement during the conduction state. The main advantage of this Zener peak clipper circuit is its low part count requirement, making it a simple, low-cost design. However, a resistor is required with the Zener diode to limit the current during the high-voltage blocking state. Moreover, the RC time constant of the element network between the resistor and the parasitic capacitances of the diodes causes a significant measurement delay, which provides insufficient bandwidth for high-frequency switching operation.

Fig. 2(b), as introduced in [28], deploys a normally-ON transistor to block the high-voltage drain bias during the

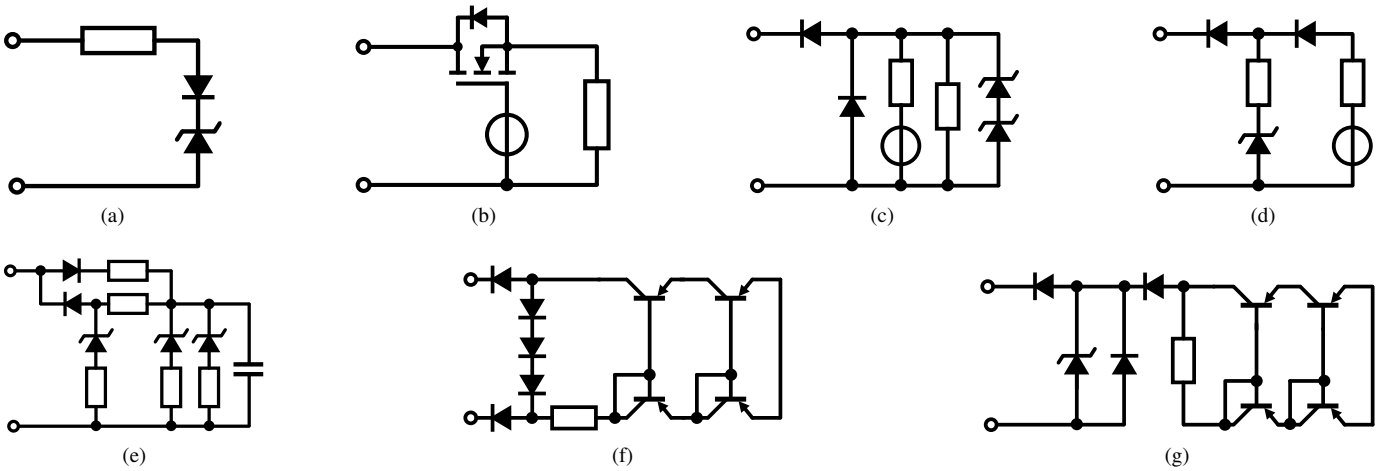


Fig. 2. Different ON-state voltage circuit topologies surveyed in prior art: (a) Zener-based, (b) MOSFET-based, (c) Resistive divider-based, (d) Dual diode-based, (e) Capacitor charge-based, (f) Current mirror-based, and (g) Current source-based (proposed).

OFF state. During the OFF transition, the voltage potential of the source terminal increases, dropping the gate-source voltage nodes below the threshold voltage of the transistor and subsequently turning OFF the device. On the other hand, when the DUT turns ON, the source terminal of the transistor decreases, causing the gate-source voltage to become higher than the threshold voltage, which subsequently turns ON the device to allow ON-state voltage measurement. Like Fig. 2(a), this circuit provides a simple design and operation. However, a large voltage overshoot can occur during the switching transitions due to the junction capacitance of the normally-ON transistor, potentially causing probe overdrive, low resolution measurement, and low accuracy. The normally-ON transistor also requires a high-voltage blocking capability to ensure safe operation when this circuit is used for high-voltage GaN HEMTs or SiC MOSFETs.

Fig. 2(c), described in [29], implements a resistive divider network along with a voltage source to provide a clamping voltage bias during the blocking state. The clamping voltage also provides a forward voltage bias for the high-voltage blocking diode during the DUT ON-state, which allows for the measurement of the ON-state resistance. The main advantage of this circuit is its fast sensing speed measurement capability through the diode discharge path during the DUT switching transitions. However, the disadvantages include the need for careful tuning of the resistive voltage divider network and Zener diodes to prevent large voltage spikes during the switching transitions. Furthermore, the design can be limited to a small range of load current operation, as it is constrained by the resistor selection.

Fig. 2(d) from [30] is implemented with two identical diodes configured in series at the input. During the DUT OFF-state, the Zener diode provides the clamping voltage bias, whereas the ON-state bias is set by the power supply with a resistor. By characterizing one of the two identical diodes, the blocking diode voltage drop caused during the DUT ON-state can be calculated and subtracted indirectly without having to sense the high-voltage node. Although this method provides precise and high-bandwidth measurement capability with a 50 Ω termination, it requires the use of a differential voltage measurement sensing mechanism. Such a mechanism, like a differential amplifier, is necessary to accurately subtract the diode voltage drop. Moreover, manufacturing variations can occur from part to part, necessitating an electrical characterization screening to ensure that the two components exhibit the same electrical behavior [31].

Fig. 2(e), which was developed in [32], [33], operates with a capacitor charging and discharging mechanism. When the DUT turns OFF, the capacitor charges via the turn-OFF path diode up to the Zener voltage. This action establishes the clamping voltage necessary for the high-voltage drain bias. When the DUT turns ON, the capacitor discharges through the turn-ON path diode while providing a voltage reference for the ON-state voltage measurement. This topology does not require a voltage supply to bias the blocking diodes. However, the circuit is prone to potentially large voltage spikes during the DUT switching transients, causing measurement overdrive. Moreover, the design requirements for charging and discharging are based on the switching voltage and current of the DUT, which requires precise tuning of the RC network and consequently restricts the operational range of the DUT to a narrow spectrum.

Fig. 2(f) shows a current mirror-based ON-resistance measurement circuit design [34]. High-voltage diodes are used to block the drain bias during the DUT OFF state while clipping the high voltage to a clamping voltage level determined by the number of diodes placed in series. When the DUT is ON, the current mirror allows current to flow through the high-voltage diodes, providing high-resolution measurement of ON-state voltage. This circuit provides high bandwidth, small measurement delay, and low noise measurement of ON-state voltage. However, a differential probe is required across the clamping diodes, making the measurement dependent on the probe selection and its specifications, such as common-mode noise rejection. In addition, a large number of parts are required, making it less ideal for a simplistic design.

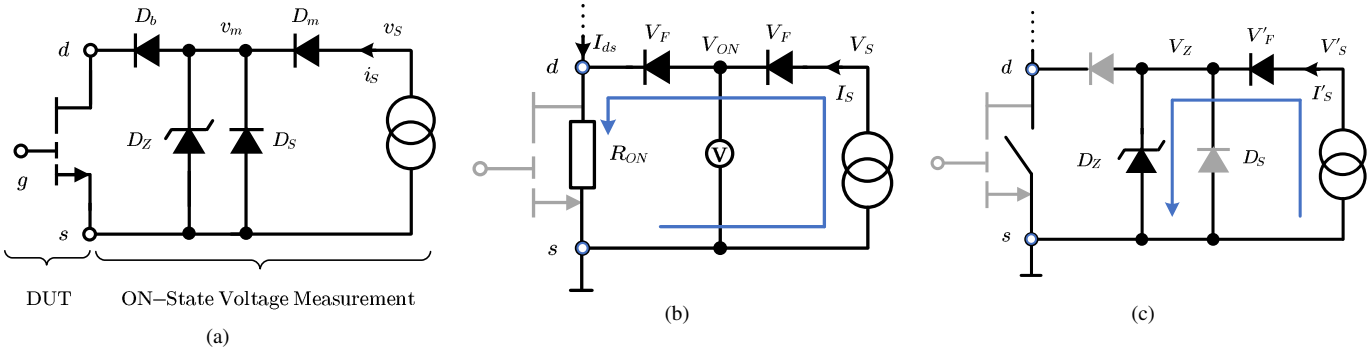


Fig. 3. The operating principle of the proposed ON-state voltage measurement circuit topology is described as follows: (a) the measurement configuration of the proposed circuit with the DUT, (b) ON-state voltage measurement biased by the current source when DUT is ON, and (c) OFF-state voltage clamped by the Zener diode, shown along with the current source path.

Fig. 2(g) shows a preview of the proposed topology, which uses a Positive-Negative-Positive (PNP) current source to drive fixed ON-OFF current amplitudes through two identical diodes [35]. Though a more detailed operation principle is described in the next section, this circuit provides fast dynamic measurement with high sensing speed, no requirement of an active probe for the diode voltage drop compensation, small voltage overshoot and undershoot, and independent from the DUT operational parameters, allowing a wide operational range across switching frequency, blocking voltage, and load current. Furthermore, a voltage compensation network is incorporated to subtract the voltage drop across the viewing diode. This network includes a 50 Ω termination connection to the measurement scope, which enables high-bandwidth measurements without the bandwidth limitations of the probe selection. Other unique topologies can also be referenced [36]–[42].

III. Proposed ON-Resistance Measurement Circuit Topology Analysis

Fig. 3(a) shows the configuration of the novel measurement circuit for the DUT. The circuit topology employs a PNP cascode current mirror framework. The current mirror is configured in such a way that it eliminates the floating ground reference issue encountered in [34]. With the proposed circuit, the clipped ON-state measurement, v_m can be measured referenced at the same ground point as the DUT source. In other words, the probe ground reference is at the same node as the DUT for measuring both v_{gs}, v_{ds}, and v_m, which is sensed across the Zener diode, D_Z. This configuration eliminates the necessity for a differential probe when measuring the ON-state of the low-side DUT. Lastly, the Schottky diode, D_S, is used to facilitate the discharge path for the blocking diode's parasitic capacitance, enabling fast sensing speed.

This circuit also uses two identical blocking diodes: one diode denoted as D_b to block the high-voltage bias from the DUT and another biasing diode, D_m, to mirror the voltage drop of the blocking diode. The blocking diode should be rated high enough to withstand the high-voltage drain bias of the DUT, whereas the mirroring diode is the same as D_b but is used as the voltage compensation reference diode to mirror the blocking diode and calculate the voltage drop across it during the ON-state. This current-driven methodology eliminates the need to sense the diode voltage with a differential operational amplifier design, as suggested in [30], due to a fixed, non-varying current set-point that is independent of the DUT load conditions. Moreover, it can provide a steady reference voltage regardless of the DUT current magnitude.

To regulate the sensitivity of the diode voltage bias to temperature fluctuations, careful selection of the operating current amplitude—aligned with a point on the forward characteristic graph that reduces the impact of temperature changes on the voltage drop across the diodes—results in optimal operating conditions. This approach ensures that the voltage drop across the diodes remains relatively stable, even in the face of temperature variations. However, this is further studied in Section IV.B: Measurement Sensitivity Error Analysis.

A. Circuit Operating Principles

Fig. 3(b) illustrates the ON-state current source path, I_s, and its operation through the diodes, D_b and D_m, which biases them at the same forward voltage drop condition: $v_{D_b}(\text{ON}) = v_{D_m}(\text{ON}) = V_F$. Here, ON defines the state when the DUT is ON, and vice versa for OFF (i.e., $v_{D_b}(\text{OFF}) = v_{D_m}(\text{OFF}) = V'_F$), which can be shown in Fig. 3(c). Fig. 3(c) describes the large-signal steady-state operation of the proposed circuit during the DUT OFF state. The high-voltage drain bias is blocked by D_b, and the voltage is clamped to the Zener voltage, V_Z, which allows high-resolution ON-state voltage measurement. In this stage, the current source will change to a smaller value, I'_s, based on the OFF-state voltage potential at V'_S, which includes the diode Zener voltage bias.

To properly understand the operating principles of the ON-state current measurement circuit, the voltage potential, v_S, during the DUT ON and OFF states needs to be calculated. The steady-state value at the node v_s changes from V_s to V'_s when the DUT is ON or OFF as follows:

$$v_s = \begin{cases} V_s = 2V_F + (I_{ds} + I_s)R_{ON}, & \text{DUT is ON,} \\ V'_s = V_Z + V'_F, & \text{DUT is OFF,} \end{cases} \quad (1)$$

where I_{ds} is the actual ON-state current through the drain and source of the DUT. The forward voltage drop of the

diode during the ON-state is denoted as $V_F = v_F(I_s)$, whereas the OFF-state forward voltage drop is expressed as $V_F' = v_F(I_s')$, depending on the current of the mirror source. The forward voltage drop of the diode can be calculated using the expression shown in (2):

$$v_F = N \cdot V_T \ln\left(1 + \frac{i_s}{I_{sat,D}}\right), \tag{2}$$

where N is the diode ideality factor, V_T is the thermal voltage, and $I_{sat,D}$ is the saturation current of the diode. The measured drain voltage, V_{ds}, is impacted by the current mirror source, i_s, as it flows through the channel in addition to the load current, I_{ds}. Therefore, V_{ds} is equal to the additional voltage drop from the added current mirror across the device ON-resistance (i.e., $V_{ds} = (I_{ds} + I_s) \times R_{ON}$).

Using the equations expressed in (1) and (2), the ON-resistance, R_{ON}, can be determined by measuring the voltage potential at v_m and subtracting the diode drop, v_F, while dividing by the total current seen by the device. This relationship is expressed in (3).

$$R_{ON} = \frac{V_m - v_F(I_s)}{I_{ds} + I_s}. \tag{3}$$

However, an accurate measurement of R_{ON} is achieved by monitoring the diode forward bias, which is dictated by the current source magnitude. The optimal ON-state value of the current mirror, I_s, requires careful tuning and consideration of various design parameters, which are further described in the next section. Once I_s is selected, the OFF-state current source magnitude, I_s', can be determined by V_s' as expressed in (4), where V_Z is the voltage of Zener diode D_Z.

$$V_s' = V_Z + V_F'. \tag{4}$$

Note that I_s' will flow through D_Z, as denoted in Fig. 3(c). The selection criteria for D_Z should be based on the power dissipation caused by I_s'.

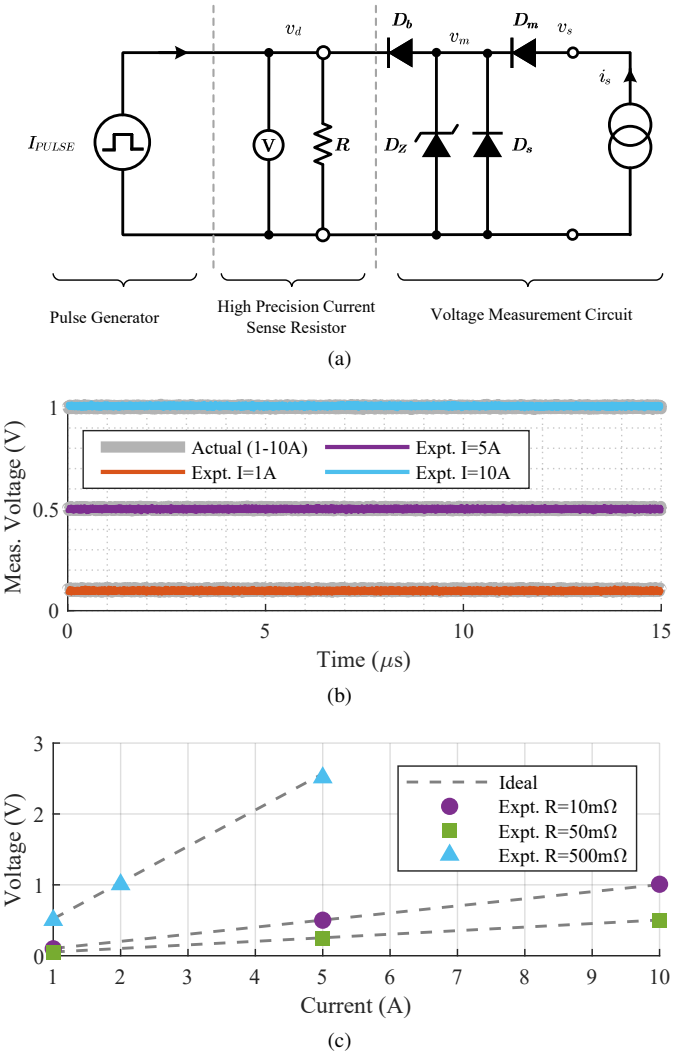


Fig. 4. Static ON-state voltage measurement experimental results describing: (a) a current pulse-based approach, incorporating a high-precision current sense resistor R followed by the proposed OVMC circuit; (b) steady-state voltage measurements across the sense resistor compared with the OVMC across a range of current pulse amplitudes of 1, 5, and 10 A with $R = 10m\Omega$; and (c) a comparison of measurement accuracy across various current and resistance values.

IV. Discussion of Static and Dynamic Measurement Experimental Results

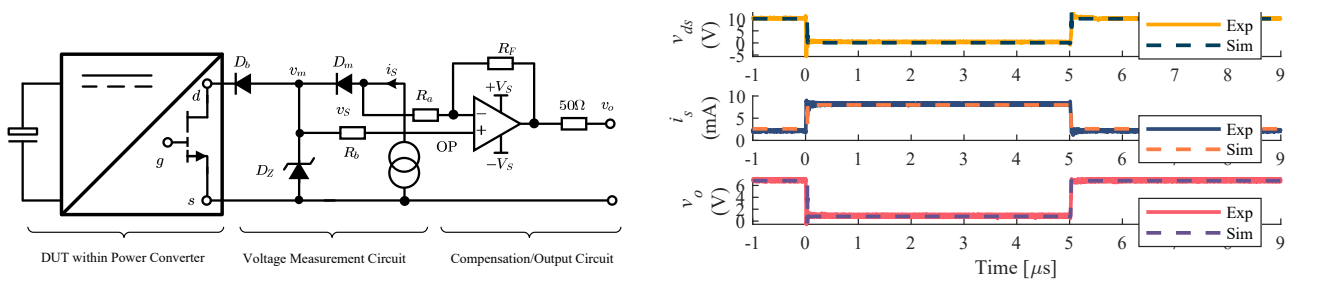
A. Static ON-State Measurements

The static measurement performance is an important aspect of the OVMC operation, as it requires precise measurement when the device is in the ON state. Fig. 4(a) illustrates the experimental setup used to measure the steady-state voltage across the resistor and to compare the OVMC performance against the ideal voltage measurement. This setup involves providing a current pulse through a high-precision load resistor and measuring the voltage across it using both a high-precision probe and the proposed OVMC. By comparing the voltage measurements from the two probes, the performance of the proposed circuit can be quantified.

Using the experimental setup shown in Fig. 4(a), the circuit's accuracy was evaluated over a range of current and load resistance values. The current pulse simulates the load current through the device, while the resistor R acts as the ON-state resistance of the DUT. The resistance values were varied between 10 mΩ, 50 mΩ, and 500 mΩ for each current pulse condition to capture a wide range of representative device resistances. Similarly, pulse current amplitudes were generated up to 10 A to represent the load current through the device.

Fig. 4(b) illustrates the steady-state measurement accuracy in the μs time domain across different current levels. The test current levels were 1 A, 5 A, and 10 A. The gray lines show the actual expected measurements, whereas the colored lines represent the measurement data from the OVMC. It can be observed that when the actual voltage measurements across the resistor are compared against the experimental results, the OVMC measurements show consistent matching with the actual values over the entire measurement time period and across a range of current amplitudes. This indicates that the forward voltage drop of the blocking diode, D_b, has been accurately subtracted via the voltage compensation network across the mirrored diode, D_m.

Fig. 4(c) depicts the measurement comparison between the



(a) (b)

Fig. 5. Dynamic (switching) ON-state voltage measurement experimental results: (a) schematic of the experimental setup of the proposed circuit measuring the DUT ON-state voltage, which is integrated into a power converter, and (b) comparison of the experimental and simulation results, highlighting the validation of the circuit operation.

ideal and the proposed OVMC experimental results across different current and resistance values. For the static measurements, the proposed circuit ensures a consistent measurement reading of up to 99% accuracy across various resistance and current values.

B. Dynamic ON-State Switching Measurements

Dynamic ON-state voltage measurements are performed in situ, capturing the behavior of the DUT while it operates in its intended switching environment. This method differs from static measurements, as it subjects the DUT to the actual dynamic stresses encountered during operation, providing a more accurate representation of its performance. The schematic illustrating the integration of the voltage measurement circuit with the power converter for dynamic testing, as well as the method for capturing the ON-state voltage of the DUT during active switching—where the DUT operates within the power conversion circuit—is shown in Fig. 5(a). The DUT used in these dynamic experiments is a 650 V, 55 A, and 55 mΩ SiC MOSFET from GeneSiC (i.e., G3F60MT06K) [43].

Fig. 5(b) illustrates a comparison between the device's measured voltage, the current from the current source, and the output from the ON-state voltage measurement circuit, presenting both experimental and simulated converter switching waveforms. There is good agreement between the experimental data and simulation results, validating the theoretical operation of the proposed circuit while demonstrating its ability to accurately measure the ON-state voltage during switching.

V. Conclusion and Future Work

In this paper, a novel circuit topology for accurately measuring the ON-resistance of WBG devices under high-voltage, fast-switching conditions has been presented. By employing a cascode current mirror configuration and a clipping circuit for high-resolution measurements during the ON-state, the proposed approach effectively addresses key challenges such as measurement accuracy, resolution, and response speed. The circuit was validated both statically and dynamically across a wide range of operating conditions, demonstrating higher resolution performance in comparison to Commercial Off-The-Shelf (COTS) solutions, as well as reduced voltage overshoot and undershoot, minimal loading effects, and high precision. Due to minimal loading impact, integration of the circuit into high-voltage conversion systems can be achieved without degrading the system or the device's switching performance, making it suitable for in-situ health monitoring of WBG semiconductors.

However, the limitations of the proposed circuit include a higher parts count compared to the topologies described in Fig. 2(a)-(d), as well as the need for careful selection and tuning of the current mirror configuration. Moreover, there is a potential performance degradation due to variations in the characteristics of the diodes and BJTs. It's important to note that mitigation strategies have been introduced and discussed extensively to address these challenges.

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