MODELING AND FABRICATING ION TRAPS FOR QUANTUM COMPUTING

Adam Masters
Ph.D. Student
Old Dominion University
Norfolk, VA USA

Dr. Sylvain Marsillac
Professor
Old Dominion University
Norfolk, VA USA

Abstract--The purpose of this project was to design, model, and fabricate the fundamental element for a 2D Quantum Computer. My aim was to design a 2D Quantum Computer based on trapped ions. Using a Paul Trap concept, I designed a surface electrode ion trap in order to trap an ion qubit. Using the COMSOL Multiphysics software, I modeled and tested various parameters, drive frequency, RF amplitude, and materials to produce an ideal scenario for fabrication. I then use the fabrication equipment available to me to create a physical representation of the model created in COMSOL.

I. INTRODUCTION

I.1 BACKGROUND

The field of quantum computing has gained momentum throughout the years as our scientific understanding of the universe has pushed classical computing to its limits. Traditionally, classical computing power can be increased by running multiple processors in parallel with each other. In order to achieve an exponential growth to computation power, the size of the computer must grow exponentially [1]. One advantage that quantum computers provide is an exponential growth in the computation power at the expensive of only a linear growth in the size of the computer.

There are several architectures available for quantum computers, with the dominant ones including trapped ions-, superconducting-, photonics- and electronic-based quantum computer. The main advantages of trapped ion quantum computers is over other architectures is their long qubit coherence times and high gate fidelities [2]. There are two main types of ion traps that are being utilized for quantum computing applications. The first is the three-dimensional linear Paul trap, traditionally made by placing four conducting rods in parallel with each other in a square pattern. Two rods opposite from each other are grounded while the other two rods have RF signals applied to them. A chain of ions can then be trapped in the middle of these four rods. These devices have deep trapping potentials but are large and present difficulty to scale up the number of trapped ion qubits [2]. Attempts have been made to fabricate three-dimensional ion traps using traditional semiconductor technology; however, the process is time-intensive and leads to other issues such as poor optical access to the ion and the incapability to shuttle the ions to perform computations [3,4]. On the other hand, surface traps have been designed as two-dimensional alternative to address the scaling issue of three-dimensional traps. While the trap depth of these designs may be smaller than their three-dimensional counterparts, experiments have shown that they can reliably trap ions for extended periods of time [5]. One appealing aspect of these traps is that they can be implemented on silicon wafers and the processes involved in making these traps are similar to the well-established processes used to fabricate microelectronics.

On top of these architectural questions, one key issue that prevents quantum computers from scaling to the point where they can exceed the computational power of classical computers is the noise levels involved within the system due notably to anomalous heating [6].

I.2 FUNCTIION(S) OF THE DESIGN

I.2.1 ELECTRIC FIELD GENERATION

The function of the design is to trap a Barium ion within the trap's geometry. In order to accomplish this, an electric field must be created above the trap surface that can be used to contain the ion. To successfully contain an ion in three dimensions, both a static and oscillating field must be utilized. The potential given by a static signal is given by:

$$\Phi_{st} = U_{DC}\left(\frac{\alpha_{DC}}{2R^2}x^2 + \frac{\beta_{DC}}{2R^2}y^2 + \frac{\gamma_{DC}}{2R^2}z^2\right) \quad (1)$$

where U_{DC} is the static voltage applied to the electrode and R is the distance between the ion and the electrode with x, y, and z being the different planes with respect to the electrode surface. According to Laplace's Theorem, $\nabla^2\Phi_{st} = 0$ implying that:

$$\alpha_{DC} + \beta_{DC} + \gamma_{DC} = 0 \quad (2)$$

and therefore, the potential in at least one direction must be non-confining. Introducing an oscillating potential gives:

$$\Phi_{RF} = V_{RF}\left(\frac{\alpha_{RF}}{2R^2}x^2 + \frac{\beta_{RF}}{2R^2}y^2 + \frac{\gamma_{RF}}{2R^2}z^2\right)cos(\Omega_{RF}t + \emptyset) \quad (3)$$

modulated at an RF frequency of Ω_{RF}. When combined

with the static potential, this leads to a linear trap with DC confinement along the z-direction and RF confinement along the x and y directions. This is to say that at time t_0, the ion can be repelled by the RF electrode and attracted to the DC electrodes. A half RF cycle later, the ion would instead by repelled by the DC electrode and attracted to the RF electrode. If the frequency of the applied RF voltage is sufficiently high, the ion would never have enough time to escape the trapping field.

I.2.2 STRONG TRAP DEPTH

The stability of the ion within the confinement field is described as the trap depth and is found through the pseudopotential equation. This is generally measured in electron volts and is on the scale of 10s to 100s of milli-electron volts for surface ion traps. If we have an oscillating electric field in the form:

$$E_{RF}(t) = -\nabla \Phi_{RF}(t) = -\nabla(\Phi_0 cos \Omega_{RF} t) \quad (4)$$

a particle of mass m located a distance r_o from the electrode will feel a force exerted from the electric field given from the equation:

$$F(t) = m\ddot{r}_0 = qE_0 \cos(\Omega_{RF} t) \quad (5)$$

Solving this equation for $r_0(t)$ gives

$$r_0(t) = -\frac{q}{m\Omega_{RF}^2} E_0 \cos(\Omega_{RF} t) \quad (6)$$

leading to a kinetic energy of

$$E_{kin,r_0}(t) = \frac{q^2}{2m\Omega_{RF}^2} {E_0}^2 \, sin^2(\Omega_{RF} t). \quad (7)$$

Ions trapped within the electric field will have two types of motion that affect their kinetic energy. The first is fast micro-motion that is induced by the RF field fluctuations. The second (slow motion) comes from stray electric fields that are present within the system. With the large timescale differences between the fast and slow micromotions, the fast motion can be thought of as a potential energy for the slow motion. With this understanding and by making the energy time-independent, the trap depth can be calculated by the pseudopotential equation:

$$\Phi_{PP} = \frac{q^2}{4m\Omega_{RF}^2} (\nabla \Phi_{RF})^2 \quad (8)$$

I.2.3 LOW BACKGROUND NOISE

With trap depths ranging from 10-150 meV, it is not difficult to introduce enough noise within the system to knock the ion out of the trapping potential region. Therefore, surface trapped ion quantum computers require the use of a cryostat, which prevents heat from within the system destabilizing of the quantum state of the ion and supplying it with enough thermal energy to leave the trap region. A second source of heat comes from Joule heating of the electrodes on the trap's surface. The equation for Joule heating is given as:

$$Q = I^2 Rt \quad (9)$$

where I is the current passing through the conductor, R is the resistance and t is the amount of time the current is applied. As current passes through any conductor, the resistance from the metal electrodes will cause them to increase in temperature and can be another source of thermal energy that can reach the ion. As such, it is important to use electrodes that are low in resistance. This can be accomplished by using metals with low resistivity values or increasing the area that the current can pass through.

A third source of noise inside the system is from dipoles that can form on the surface of any dielectric. The lasers energy used to control the motion and quantum state of the trapped ion can be as high as 3 eV. When the cooling lasers hit the trapped ion, photons will deflect off the ion and can hit any surface within the cryostat. At 3 eV, the photon has enough energy to excite the material through the photoelectric effect. The most common materials inside the cryostat that can form a dipole are the optical windows of the cryostat, and oxide that forms on the surface of the electrodes, and the material exposed between electrodes. As the strength of the dipole increases, the location of the ion within the trap will change. This can cause the ion to move out of sight of the cooling lasers, preventing them from creating a quantum state within the ion. As designs improve over time, these ions are trapped closer to the surface, making these effects of greater importance.

I.2.4 LOW POWER SUPPLY DEMAND

All surface ion traps will have some inherent capacitance value that is seen by the power supply. At the high frequencies ranges that are used for trapping ions, this capacitance can place a high demand on the power supply; so, keeping the capacitance low is ideal. The main source of capacitance in a surface ion trap is from the gap between the RF and DC electrodes. Figure 1 shows an illustration of the cross-section between two electrodes as well as the generalized equation for calculating capacitance. The easiest way to minimize the capacitance would be to have a large separation, d, between the electrodes and also make them as thin as possible to reduce the surface area, A, that they see. The

dielectric constant, ε, used here is generally the one for vacuum ($\varepsilon=\varepsilon_0$).

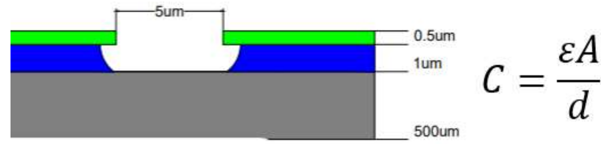

Figure 1: (Left) Illustration of electrode separation detailing the values that contribute to trap capacitance. (Right) Equation used to calculate capacitance between electrodes.

As mentioned earlier, the problems with having a large gap between the electrodes is that it exposes more material to scattered laser light that can cause dipole charging. Reducing the thickness of the electrodes will also increase their resistance, which increases the Joule heating. Both of these issues contribute to difficulty in trapping an ion as the ion-to-electrode distance is decreased.

One solution to this problem is to create an impedance matching network as well as a resonator. These two systems will work together to help resolve some of the losses associated with the trap capacitance and also help amplify the voltage signal from the power supply without causing an increase demand on the equipment.

II. Design approach

The fabricated surface ion trap quantum computer should be expected to trap an ion with a lifetime that is sufficiently long enough to perform basic quantum computing tasks. As such, it is expected to have minimized noise within the system that could cause the ion to lose its quantum state.

II.1 Details of the engineering design

The use of COMSOL Multiphysics allowed for the initial designs to be tested for capacitance as well as trap height and depth. I was also able to experiment with electrode thickness, drive frequency and RF and DC voltage values that would maximize the trapping potential. Once a design was shown to have good characteristics, fabrication on the design took place in the microelectronics laboratory at Old Dominion University. This device was then characterized using C-V and I-V measurements facilitated by LabVIEW software in communication with a Keithley 590 CV analyzer and Keithley 2400 source meters.

II.1.1 COMSOL Multiphysics simulation

To get an idea of how my initial design would perform, I built a 3D model inside COMSOL as shown in Figure 2. The design consisted of a center DC/ground electrode, two RF electrodes and six other DC electrodes that are used to control the location of the ion as well as provide trapping potential in the y-direction. The three center electrodes all have a width of 120 µm and are separated by a 5 µm gap. The outer DC electrodes are spaced 13 µm from each other as well as from the RF electrodes.

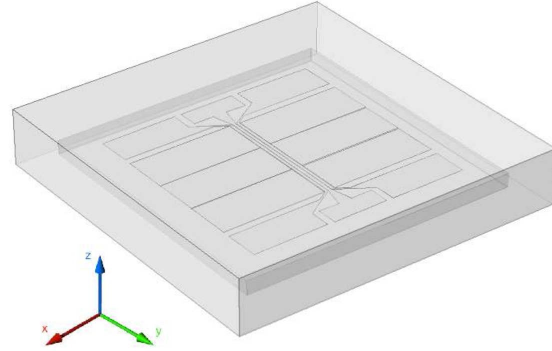

Figure 2: 3D Model of the ion trap that was loaded into COMSOL for simulating trap height, depth and capacitance.

Once the model was built, I placed a 1V potential on the RF electrodes and held all other electrodes at 0V. This allowed me to see the trapping potential that an ion would see as it passes above the surface of the trap. I could then scale this data to find the actual trap height and depth for any voltage applied to the electrodes. Figure 3 shows a cross-sectional view of the trap potential along the x- and z-axes.

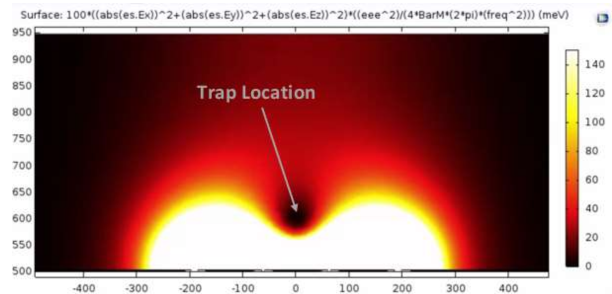

Figure 3: COMSOL simulation output showing location of ion trapping site.

As great as COMSOL can be at simulating multiphysics problems, it is not always able to give the exact values that are required to determine the trap characteristics that are needed. As such, the solution to this simulation had to be exported and the data was analyzed using a MATLAB code that I wrote. This code was designed to find a local minimum value (the location of the ion trap) and search outward until it found a local maximum in all directions. The lowest of these maximum values would be the trap depth for any given

voltage applied to the RF electrodes. Using the design shown, I found *this trap depth to be 30 meV*. While this is not a very strong trapping potential, it is sufficient to trap an ion in the equipment I have available to me. A simulation of the capacitance using this design was also performed in COMSOL and the value was found to be *54 pF when the electrodes are supplied with a 1 MHz signal*.

II.1.2 FABRICATION PROCESS

The ion traps were fabricated on standard 2" round silicon wafers. The dimensions for the ion trap are 10 mm x 10 mm which allows multiple traps to be created on each silicon wafer. In total, there were 8 fabrication process steps required to create ion traps on the wafer. The steps are shown in Figure 4 below. A general discussion of how these steps were performed also takes place in the following sections.

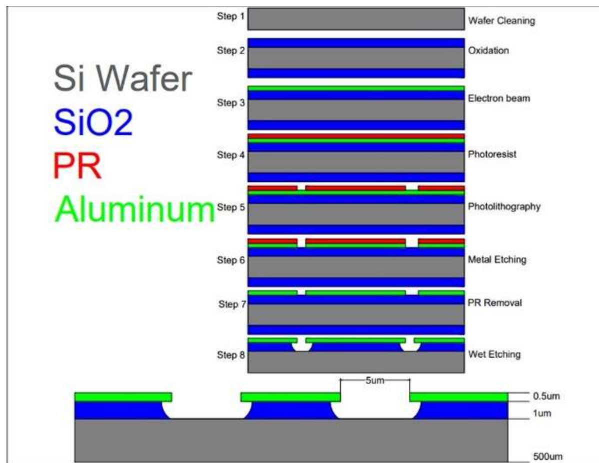

Figure 4: 8-step process used to fabricate the surface ion trap.

II.1.2.1 WAFER CLEANING

Wafer cleaning is an important initial step in any fabrication process. Because the smallest feature size on these traps is only 5 µm, a single piece of dust or fingerprint can cause the lithography process to fail. Following the standard procedure for silicon wafer cleaning, the wafers were first rinsed with deionized water to remove any loosely bonded surface contamination. This was then followed by a 1-minute soak in a mixture of sulfuring acid and hydrogen peroxide. The solution was preheated to 120°C and placed in an ultrasonic bath. This process removes any organic material from the surface of the wafer. A final soak in hydrofluoric acid removes any native oxide buildup on the surface of the wafer. The wafers are then given a final rinse in deionized water to remove any excess acid and dried with a nitrogen gun.

II.1.2.2 OXIDATION

An oxide layer was formed on top of the cleaned wafers using a dry-wet-dry thermal oxidation process. The purpose of this layer is to create an electrically insulating layer between the metal electrodes. This was accomplished by heating the furnace to a temperature of 1100°C. The wafers were placed on a quartz wafer boat and slowly pushed into the center of the furnace over the course of 1 minute. Ultra-high purity oxygen was flowed into the furnace at a rate of 1.2 lpm for 10 minutes to create an initial dry oxide layer. The process was then switched to a wet oxidation process where deionized water was heated to a temperature of 95°C in a flask bubbler. Nitrogen was pushed through the flask at a rate of 0.3 lpm to force the steam into the furnace. This process was allowed to continue for 6 hours to build the bulk oxide layer. A final 10-minute dry oxidation process then took place.

II.1.2.3 ELECTRON BEAM METALLIZATION

Our lab has facilities to create metal layers using physical vapor deposition (PVD). The PVD methods available are thermal evaporation, electron-beam evaporation, and sputtering. Due to the higher quality films and a well-established process, I decided to use electron-beam evaporation for this step. A 10kV potential was placed across the tungsten filament, heating it and causing electrons to free themselves through thermionic emission. These electrons are then re-directed via an electromagnetic field (Lorentz force) inside the vacuum chamber and collide with the aluminum pellets inside of the crucible. A loss of kinetic energy during each collision causes the metal to heat until it evaporates. After 15 minutes of aluminum evaporation, a 0.5 µm layer of aluminum was deposited across the entire surface of the wafer.

II.1.2.4 PHOTORESIST APPLICATION AND PHOTOLITHOGRAPHY

A very critical and limiting step within the fabrication process is photolithography. This is the method by which the electrodes are patterned on the wafer surface from the solid aluminum film that was created during the metallization process. The lab I was using has a Heidelberg uMLA Maskless Aligner. This system uses a 365 nm LED light source passing through a digital micromirror device (DMD). The DMD allows precise control over what sections of the wafer are illuminated during the photolithography process. The pattern shown in Figure 5 is the design that performed well in COMSOL and also had ease-of-use in my lithography process. The red sections are the areas where the metal contacts would be and all the areas in white are where light would be exposed during the lithography process.

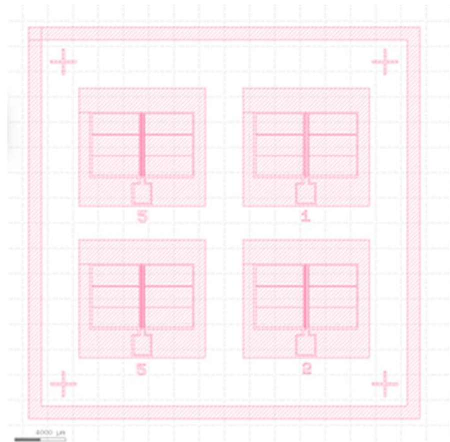

Figure 5: 2D K-Layout model that was imported into the Heidelberg µMLA system for photolithography purposes.

Prior to being inserted into the uMLA, AZ-1512 positive photoresist was applied to the wafer surface through spin-coating at 4500 rpm for 30 second. This gives a consistent 1.1 µm layer of photoresist over the wafer surface. A prebake at 105°C for 1 minute then followed. The wafer was then loaded into the uMLA, and the pattern was placed on the photoresist. A post bake at 105°C for 1 minute was performed.

After exposure in the uMLA, the wafer was then placed into AZ-400K developer to remove any section of photoresist that were exposed to light in the uMLA. This would leave the red sections in Figure 5 still on the wafer and all the white sections would be where the photoresist is removed. Once the photoresist was patterned using photolithography, the materials under the photoresist can be patterned using wet etching processes. Any areas where photoresist remained would be used to protect the materials underneath from the effects of the subsequent wet etching steps.

II.1.2.5 Metal Etching

The type of wet etchant used depends on the material that is to be removed. In this case, I had aluminum electrodes that I wanted to etch away so the most common wet etchant is a mixture of phosphoric, nitric, and acetic acids. This solution was able to etch through the metal in 10 minutes, while being agitated by a magnetic stir stick spinning at 300 RPM. The results of the metal etching can be seen in Figure 6. These results will be further discussed in the characterization section.

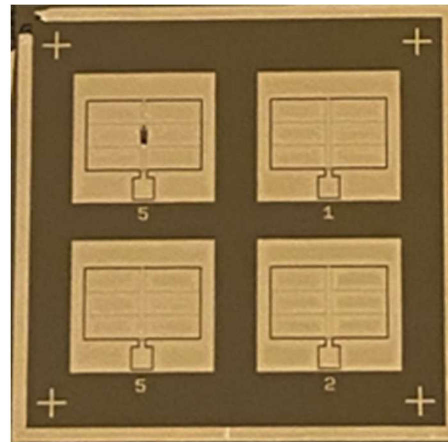

Figure 6: Optical microscope image of the surface ion traps after metal etching. The numbers below the traps indicate the RF to DC electrode separation distances in micrometers.

II.1.2.6 Oxide Etching

A final step that I took during my fabrication process was to etch through the oxide layer that was underneath the electrodes. This was done for two reasons. First is that this allows to eliminate the insulation SiO_2 layer that would be between the electrodes. This helps reduce the amount of dipole charging effect that can occur as laser light is scattered across the surface of the trap. Secondly is that it increases the distance that the electrical signal must pass through before the electrodes see each other. This helps further reduce the capacitance, as discussed earlier. Wet etching of silicon dioxide is a very well understood process in the microelectronics industry and is carried out by a buffered oxide etchant (BOE) solution. BOE is a mixture of hydrofluoric acid and ammonium fluoride. The buffering agent allows a very stable etching rate every time the solution is used. This solution has an etching rate of approximately 120 nm/min at room temperature, so the etching time for my device was around 8 minutes.

III. Device Characterization

Device characterization is important to perform before placing the trap into the system because it will provide useful information that can tell you if you had a successful fabrication or not. I also had traps with three different electrode separation dimensions and learning how this parameter effects the trap performance was also important in understanding how to improve future iterations of the design.

III.1 Optical Microscopy

Optical microscopy was used to visually look at the separation between the electrodes to ensure the photolithography process was properly carried out. Figure 7 shows images of the 1- 2- and 5-µm electrode separations. It can be seen that the 1 µm separation

between the electrodes was not successful, requiring further refinement of the photolithography process if these separations are found to be necessary for future studies. There was complete separation between the electrodes when 2 and 5 µm separation was desired. A defect occurred in one of the 5 µm traps, which made it unsuitable for further characterization. Defects of this nature are typically caused by surface contamination that may not have been fully removed during the wafer cleaning process.

III.2 SCANNING ELECTRON MICROSCPOY (SEM)

SEM images were taken by cleaving one of the traps across the electrode separation plane. This allowed me to take images of the trenches that were formed during the metal and oxide wet etch processes. A 2000x magnification was used which allowed capturing of a full electrode separation trench as shown in Figure 8. It is seen that successful electrode separation was accomplished as well as the desired metal overhangs that were illustrated Figure 4. These overhangs provide the additional benefit of blocking scattered laser photons from hitting the wafer surface and degrading performance of the ion trap.

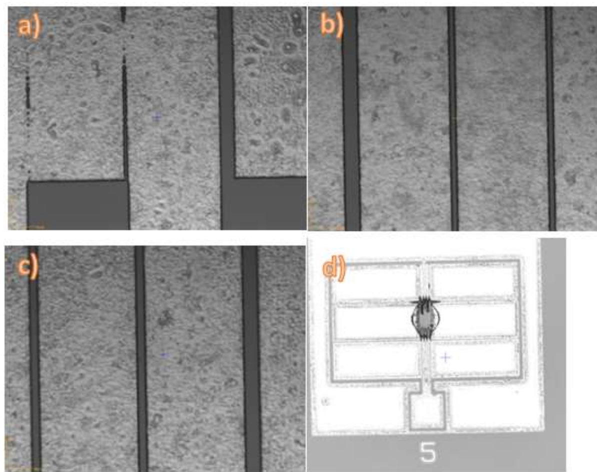

Figure 7: Optical microscope images showing of the ion traps. a) Shown that the process can use further refinement in order to achieve 1 µm resolution. b & c) 2 and 5 µm electrode separation were successful. d) A defect occurred during the fabrication of one of the 5 µm traps.

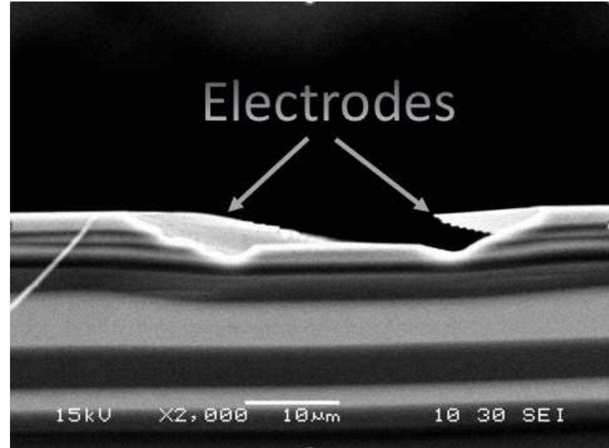

Figure 8: SEM image of one of the electrode separation trenches. It is seen that the trench was etched to a sufficient depth and the electrode was able to suspend itself above a portion of the trench.

III.3 ELECTRICAL PROPERTIES

Two electrical characterization tests were performed to verify that the trap fabrication and COMSOL simulation were successful, nominally C-V measurements and I-V measurements between the RF and DC electrodes. The C-V measurements were taken using the previously described Keithley equipment and was found to be around 90 pF for both the 2 and 5 µm electrode separation. While this is higher than the 54 pF results found with the COMSOL simulations, the design had changed slightly due to fabrication limitations. It is also possible that the material properties that were used in COMSOL did not exactly match the material properties of the actual trap. The results are shown in Figure 9.

One initial concern was that there was no noticeable difference in the capacitance values when the electrode separation was changed. After further analysis, the portion of the electrodes that contribute to capacitance is very small in the section where the separation was change compared to the capacitance that was given across the entire electrode surface. This means that further reducing the electrode separation gap can be safely performed without pushing the capacitance about the power supply’s capabilities.

I-V measurements were also taken between the RF and DC electrodes using the Keithley 2400 source meter. This test was performed to verify that there was sufficient electrical separation between the electrodes. Both 2 and 5 µm electrode separation showed resistance values in the MΩ range. The results for this test are shown in Figure 10. Resistance values in this range ensures that proper electrical insulation is present between the two electrodes.

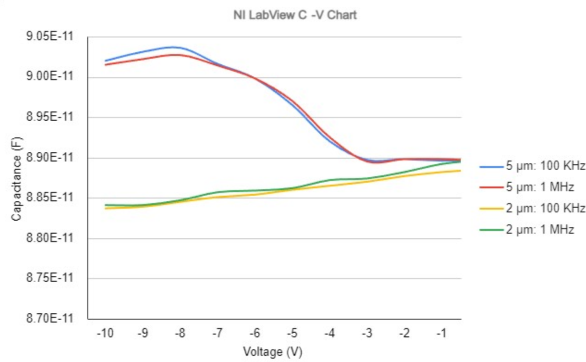

Figure 9: CV Measurement results from the ion traps with 2 and 5 µm electrode separation. Tested frequencies of 100 kHz and 1 MHz.

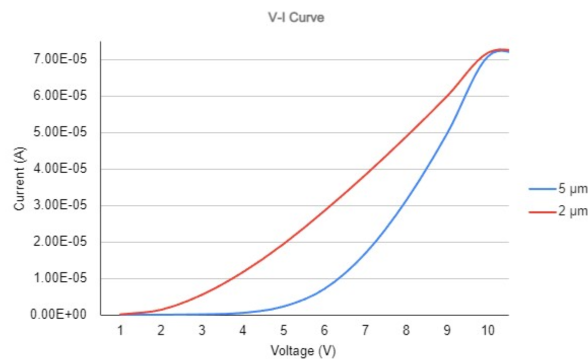

Figure 10: I-V Measurements taken between the DC and RF electrodes on traps with 2 and 5 µm electrode separation.

IV. Conclusion

I was able to successfully model and fabricate surface ion traps using traditional microelectronic fabrication techniques. Optical microscopy as well as scanning electron microscopy showed full electrode separation of the RF and DC electrodes for traps with 2 and 5 µm separation. This was also verified through I-V testing between the electrodes. With further refinement to the process, it should be possible to reduce the electrode separation to 1 µm. This would be beneficial in reducing the dipoles that can be created on the silicon surface from laser scattering. C-V tests have shown that reduction in electrode separation plays a minimal role in the capacitance values of the trap and therefore no additional load is placed on the power supply, making investigation into smaller electrode separation an ideal candidate for future projects.

V. References

[1] E. Rieffel and W. Polak, "An Introduction to Quantum Computing for Non-Physicists" ACM Inc, New York, 2000.
[2] https://aip.scitation.org/doi/10.1063/1.5088164.
[3] D. Cho, S. Hong, M. Lee and T. Kim, "A review of silicon microfabricated ion traps for quantum information procesing" Micro and Nano Systems Letters, vol. 3, no. 2, 2015.
[4] G. Wilpers, P. See, P. Gill and A. Sinclair, "A monolithic array of three-dimensional ion traps fabricated with conventional semiconductor technology" Nature Nanotechnology, 2012.
[5] M. e. a. Niedermayr, "Cryogenic surface ion trap based on intrinsic silicon," New Journal of Physics, vol. 16, 2014.
[6] S. Wang, E. Fontana, M. Cerezo, K. Sharma, A. Sone, L. Cincio and P. Coles, "Noise-induced barren plateaus in variational quantum algorithms" Nature Communications, vol. 12, 2021.